In the drawings:

Figure 2 has been amended to change the block labeled "C_2 214" to "C_1 214".

Remarks

Applicant respectfully requests reconsideration of this application as amended. The specification has been amended to correct minor informalities. Figure 2 has also been amended to correct a minor informality. Claims 3-5, 7 and 20 have been amended. Claims 25-31 have been added. Claims 8-13 have been cancelled. Claims 1-2, 14-19, and 23-24 were previously cancelled. Therefore, claims 3-7, 20-22, and 25-31 are presented for examination.

35 U.S.C. §112 Rejection

Claims 9 and 11 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 9 and 11 have been cancelled. Therefore, the 35 U.S.C. §112 rejection has been obviated.

35 U.S.C. §102(b) Rejection

Claims 3-5, 8-9, 12-13 and 20-22 stand rejected under 35 U.S.C. §102(b) as being anticipated by Liong et al. (U.S. Patent No. 5,784,548). Applicant submits that the present claims are patentable over Liong.

Liong discloses a battery backup mirrored cache memory module for a cache dynamic random access memory (DRAM) system that senses the Vcc level supplied through the cache controller to the cache memory. If the cache controller supplied Vcc falls below a present threshold, the battery backup apparatus switches the cache memory array to a backup battery Vcc source and a backup refresh control generator unit that is also powered by the backup battery Vcc source. Cache memory reliability is further enhanced by providing two cache

memory banks that are accessed simultaneously using a common address and have a stored parity bit with each data entry. When a read access is made, a cache memory bank selector selects one of the bank's output data if no parity error is detected. If one bank has a parity error, the other bank's output can be used to correct the data in the bank with the parity error. (Liong at Abstract.)

Claim 3, as amended, recites:

> A method comprising:
> reading data from a first dirty cache line in a cache memory;
> determining if the data within the first dirty cache line is corrupt;
> marking the first dirty cache line invalid if the data within the first dirty cache line is corrupt;
> determining if a duplicate cache line of the first dirty cache line exists, wherein duplicate cache lines are only created for dirty cache lines in the cache memory;
> if the duplicate cache line exists:
> writing data within the duplicate cache line to a first location in a memory if the data within the duplicate cache line is not corrupt; and
> marking the first dirty cache line available.

Applicant submits that Liong does not disclose or suggest determining if a duplicate cache line of the first dirty cache line exists, wherein in the cache memory duplicate cache lines are only created for dirty cache lines, as recited by claim 3. Liong discloses providing two cache memory banks that may be accessed simultaneously and may be used to correct data in a memory bank. However, Liong does not disclose or suggest determining if a duplicate cache line of a dirty cache line exists, ***where duplicate cache lines are only created for dirty cache lines in the cache memory***. Therefore, claim 3 is patentable over Liong.

Claims 4-7 and 25-27 depend from claim 3 and include additional limitations. Therefore, claims 4-7 and 25-27 are also patentable over Liong.

Independent claim 20 also recites, in part, determining if a duplicate cache line of the first dirty cache line exists, wherein in the cache memory duplicate cache lines are only created for dirty cache lines. As discussed above, Liong does not disclose or suggest such a feature. Therefore, claim 20 is patentable over Liong for the reasons discussed above with respect to claim 1. Claims 21, 22, and 28-31 depend from claim 20 and include additional limitations. As such, claims 21, 22, and 28-31 are also patentable over Liong.

35 U.S.C. §103(a) Rejection

Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Liong et al. (U.S. Patent No. 5,784,548). Claim 11 has been cancelled, thus obviating the present rejection.

Claims 6, 7, 10 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Liong et al. in view of Loechel (U.S. Patent No. 5,895,485). Claims 10 and 13 have been cancelled. Applicant submits that claims 6 and 7 are patentable over Liong in view of Loechel.

Loechel discloses a method for mirroring cache data from a first controller to an alternate controller in a data storage system, where the data storage system includes a host computer connected to the first controller and the alternate controller. (Loechel at Abstract.) Claims 6 and 7 depend from independent claim 3 and include additional limitations. As discussed above with respect to claim 1, Liong does not disclose or suggest determining if a duplicate cache line of the first dirty cache line exists, wherein in the cache memory duplicate cache lines are only created for dirty cache lines. Furthermore, applicant can find no disclosure or suggestion in Loechel of such a feature. Therefore, claims 6 and 7 are patentably distinguished from Liong in view of Loechel.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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